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Description

[CIRCUIT AND METHOD FOR ENHANCING MOTION PICTURE QUALITY]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92124166, filed September 02, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] This invention generally relates to a driving circuit and method for a display, and more particularly to a circuit and method for enhancing motion picture quality.

[0004] Description of Related Art

[0005] After the liquid crystal was discovered, it has been applied to display devices and other applications. For motion picture display applications, the liquid crystal display (LCD) has the advantages of being light, compact and lower radiation compared to the traditional CRT display and

therefore a better choice over the traditional CRT display. A LCD includes a plurality of pixels. The liquid crystal is filled between two substrates. The transmission rate of the liquid crystal then can be changed by applying a voltage on the electrodes on the substrates. Because the liquid crystal is filled between two electrodes, it can be a so-called a liquid crystal capacitor. FIG. 1 is a pixel 100 of a conventional LCD. The thin film transistor (TFT) 130 is controlled by the scan signal 104 to determine whether or not to introduce the image signal 102. The storage capacitor 120 stores the image signal 102 so that it can supply the driving voltage to the liquid crystal capacitor 110 even if the TFT 130 is off. Because the capacitance of the liquid crystal capacitor 110 depends on the direction of the liquid crystal, when the voltage is applied to change the direction of the liquid crystal, the capacitance of the liquid crystal capacitor 110 is also changed.

[0006] FIG. 2 shows the relationship between the voltage applied to the liquid crystal capacitor of a pixel |V| and the frame time. The voltage is changed after the nth frame and requires several frames to reach the target voltage. Before the voltage 220 of the liquid crystal capacitor reaches the target voltage 210, this pixel will show an unanticipated

gray level for a short period of time. FIG. 3 shows the relationship between the gray level and the frame time for a pixel. As shown in FIG. 3, the pixel is going to change from Black to a target gray level 310 at the nth frame. Due to the characteristics of the liquid crystal, it takes several frames to reach the target gray level 310.

[0007] The aforementioned response delay may not be a serious issue for a still image application. However, for a motion picture application, this delay causes a poor quality of the image. Conventionally, the delay can be improved by applying a compensation voltage when changing the voltage applied to the electrodes so that the voltage on the liquid crystal capacitor |V| is higher than the target voltage. Then the voltage applied on the liquid crystal capacitor become normal at the next frame. FIG. 4 shows the conventional method to improve the response delay on the LCD. The voltage |V| is changed at the nth frame and a compensation voltage 430 is also applied so that the voltage 420 of the liquid crystal capacitor can reach the target voltage 410 within the nth frame. FIG. 5 shows the relationship between the gray level and the frame time for a pixel after the conventional method is applied. As shown in FIG. 3, the pixel changes from Black to a target gray

level 510 within the nth frame. The voltage 420 of the liquid crystal capacitor can reach the target voltage 410 within the nth frame and without waiting for several frames.

[0008] The conventional method for enhancing the motion picture requires comparing a frame data of the previous frame and the frame data of the present frame. If the frame data in the previous frame are different from that of the present frame, a compensation voltage is applied; otherwise, no compensation is applied. This conventional method requires a frame memory to store the frame data of the previous frame. When the frame data of the previous frame is outputted, the frame data of the present frame will be saved. One also can use two frame memory devices to store the frame data of the previous frame and the frame data of the present frame. To reduce the costs, a prior art has been proposed (Taiwan Patent No. 513685 and its corresponding US Patent No. 2002/0180676) to enhance the motion picture quality. This prior art requires a complex and precious timing control and uses four single-port buffers to store the frame data of the previous and present frames at the same time. To prevent conflict of reading and writing in the prior art , bigger memory

devices are required. Further, although the prior art uses a single frame memory to store the frame data of the previous frame, practically the frame memory is still very expensive. Hence, how to reduce the size of the frame memory is an important issue to be concerned.

SUMMARY OF INVENTION

[0009] An object of the present invention is to provide a circuit and method for enhancing motion picture quality to reduce the data of the frame thereby reducing the size of the frame memory.

[0010] Another object of the present invention is to provide a circuit and method for enhancing motion picture quality to save the frame data partially and alternately thereby reducing the size of the frame memory.

[0011] Still another object of the present invention is to provide a circuit and method for enhancing motion picture quality by using two dual-port buffers to simplify the timing control of the frame memory.

[0012] The present invention provides a circuit for enhancing motion picture quality, comprising: a first dual-port buffer for receiving and temporarily storing a first frame data, and first-in-first-out outputting the first frame data; a second dual-port buffer for receiving and temporarily

storing a second frame data, and first-in-first-out outputting the second frame data; the first frame data being shown in a motion picture after the second frame data; a frame memory for storing a motion picture data; a multiplexer unit, coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data to said second dual-port buffer; and a signal converter for obtaining a compensation data to output a third frame data in response to the first frame data and the second frame data corresponding to the first frame data.

[0013] In a preferred embodiment of the present invention, the circuit further comprises: a first data latch for receiving a fourth frame data and outputting the first frame data, wherein the number of bits of the first frame data is larger than the number of bits of the fourth frame data; a second data latch for receiving a fifth frame data and outputting the second frame data, wherein the number of bits of the second frame data is larger than the number of bits of the fifth frame data; wherein the signal converter obtains the compensation data to output the third frame data in re-

sponse to the fourth frame data and the fifth frame data corresponding to the second frame data.

[0014] In a preferred embodiment of the present invention, the circuit further comprises a nonlinear quantizer for receiving a sixth frame data and quantizing the sixth frame data by using a nonlinear quantization method to output the fourth frame data, wherein the signal converter is for receiving the sixth frame data and compensating the sixth frame data based on the compensation data to obtain the third frame data.

[0015] The present invention provides a circuit for enhancing motion picture quality, comprising: a nonlinear quantizer for receiving a first frame data and quantizing the first frame data by using a nonlinear quantization method to output a second frame data; a frame memory module, coupled to the nonlinear quantizer, for receiving the second frame data and outputting a third frame data corresponding to the second frame data, the second frame data being shown in a motion picture after the third frame data; and a signal converter, in response to the second frame data and the third frame data corresponding to the second frame data, for obtaining a compensation data to compensate the first frame data for outputting a fourth

frame data.

[0016] In a preferred embodiment of the present invention, the frame memory module comprises: a first dual-port buffer for receiving and temporarily storing the second frame data, and first-in-first-out outputting the second frame data; a second dual-port buffer for receiving and temporarily storing the third frame date, and first-in-first-out outputting the third frame data; a frame memory for storing a motion picture data; and a multiplexer unit coupled to said first dual-port buffer, said second dual-port buffer and said frame memory; for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said third frame data to said frame memory to said second dual-port buffer.

[0017] In a preferred embodiment of the present invention, the signal converter comprises: a motion picture enhancing unit for simultaneously receiving the second frame data and the third frame data and comparing the second frame data and the second frame data to generate the compensation data based on the difference between the second frame data and the third frame data; and a data processing unit for simultaneously receiving the first frame data and the compensation data corresponding to the first

frame data, and compensating the first frame data based on the compensation data to obtain the fourth frame data.

[0018] The present invention provides a method for enhancing motion picture quality, comprising: providing a first dual-port buffer, a second dual-port buffer, and a frame memory; using the first dual-port buffer to receive and temporarily store a first frame date, and first-in-first-out outputting the first frame data; using the second dual-port buffer to receive and temporarily store a second frame date, and first-in-first-out outputting the second frame data; the first frame data being shown in a motion picture after the second frame data; using the frame memory to store a motion picture data; multiplexing said motion picture data in said frame memory thereby selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data to said second dual-port buffer; and obtaining a compensation data to output a third frame data in response to the first frame data and the second frame data corresponding to the first frame data.

[0019] The present invention provides a circuit for enhancing motion picture quality, comprising: a first dual-port buffer for receiving and temporarily storing a first frame date,

and first-in-first-out outputting the first frame data; a second dual-port buffer for receiving and temporarily storing a second frame date, and first-in-first-out outputting the second frame data; the first frame data being shown in a motion picture after the second frame data; a frame memory for storing a motion picture data; a multiplexer unit, coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data to said second dual-port buffer; a signal converter, in response to the first frame data, a third frame data, and the second frame data corresponding to the third frame data, for obtaining a compensation data to output a fourth frame data and a fifth frame data; a first data flow switcher receiving a sixth frame data and a seventh frame data and transforming the sixth frame data and the seventh frame data into one of the first frame data and the third frame data respectively and the third frame data and the first frame data respectively; and a second data flow switcher for receiving the fourth frame data and the fifth frame data and transforming the fourth frame data and the fifth frame data into one of the eighth

frame data and the ninth frame data respectively and the eighth frame data and the ninth frame data respectively.

[0020] In a preferred embodiment of the present invention, the circuit further comprises a first data latch, coupled to and between the first data flow switcher and the first dual-port buffer, the first data flow switcher receiving the sixth frame data and the seventh frame data, and transforming the sixth frame data and the seventh frame data into one of a tenth frame data and the third frame data respectively and the third frame data and the tenth frame data respectively, the first data latch for receiving the tenth frame data and outputting the first frame data, the number of bits of the first frame data is larger than the number of bits of the tenth frame data; a second data latch, coupled to and between the first dual-port buffer and the signal converter, receiving the second frame data and outputting an eleventh frame data, the number of bits of the second frame data is larger than the number of bits of the eleventh frame data; wherein the signal converter, in response to the tenth frame data, the third frame data, and the eleventh frame data corresponding to the third frame data, obtaining the compensation data to output the fourth frame data and the fifth frame data.

[0021] In a preferred embodiment of the present invention, the circuit further comprises: a first nonlinear quantizer, coupled to and between the first data flow switcher and the first data latch, the first data flow switcher for receiving the sixth frame data and the seventh frame data, and transforming the sixth frame data and the seventh frame data into one of a twelfth frame data and the third frame data respectively and the third frame data and the twelfth frame data respectively, the first nonlinear quantizer for receiving the twelfth frame data and quantizing the twelfth frame data by using a nonlinear quantization method to output the tenth frame data; and a second nonlinear quantizer, coupled to and between the first data flow switcher and the signal converter, receiving the third frame data and quantizing the third frame data by using a nonlinear quantization method to output the thirteenth frame data; wherein the signal converter, in response to the twelfth frame data, the third frame data, and the thirteenth frame data corresponding to the eleventh frame data, obtains the compensation data to output the fourth frame data and the fifth frame data.

[0022] The present invention provides a circuit for enhancing motion picture quality, comprising: a first nonlinear quan-

tizer for receiving a first frame data and quantizing the first frame data by using a nonlinear quantization method to output a second frame data; a second nonlinear quantizer for receiving a third frame data and quantizing the third frame data by using a nonlinear quantization method to output a fourth frame data a frame memory module, coupled to the first nonlinear quantizer, for receiving the second frame data and outputting a fifth frame data corresponding to the second frame data, the second frame data being shown in a motion picture after the fifth frame data; a signal converter, in response to the first frame data, the third frame data, the fourth frame data and the fifth frame data corresponding to the fourth frame data, for obtaining a compensation data to output a sixth frame data and a seventh frame data; a first data flow switcher for receiving an eighth frame data and a ninth frame data and transforming the eight frame data and the ninth frame data into one of the first frame data and the third frame data respectively and the third frame data and the first frame data respectively; and a second data flow switcher for receiving the sixth frame data and the seventh frame data and transforming the sixth frame data and the seventh frame data into one of the tenth

frame data and the eleventh frame data respectively and the tenth frame data and the eleventh frame data respectively.

[0023] In a preferred embodiment of the present invention, the frame memory module comprises: a first dual-port buffer for receiving and temporarily storing the second frame date, and first-in-first-out outputting the second frame data; a second dual-port buffer for receiving and temporarily storing the fifth frame date, and first-in-first-out outputting the fifth frame data; a frame memory for storing a motion picture data; and a multiplexer unit coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory; for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said fifth frame data to said second dual-port buffer.

[0024] The present invention provides a method for enhancing motion picture quality, comprising: providing a first dual-port buffer, a second dual-port buffer, and a frame memory; using the first dual-port buffer to receive and temporarily store a first frame date, and first-in-first-out outputting the first frame data; using the second dual-port buffer to receive and temporarily store a second

frame date, and first-in-first-out outputting the second frame data; the first frame data being shown in a motion picture after the second frame data; using the frame memory to store a motion picture data; multiplexing said motion picture data in said frame memory thereby selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data to said second dual-port buffer; and obtaining a compensation data to output a fourth frame data and a fifth frame data, in response to the first frame data, a third frame data, and the second frame data corresponding to the third frame data; transforming a sixth frame data and a seventh frame data into one of the first frame data and the third frame data respectively and the third frame data and the first frame data respectively, in response to a time sequence; and transforming the fourth frame data and the fifth frame data become one of an eighth frame data and a ninth frame data respectively and the ninth frame data and the eighth frame data respectively, in response to the time sequence.

[0025] The present invention uses a memory structure including a frame memory and two dual-port buffers. The memory structure can read the frame date of the previous frame

and store the frame date of the present frame at the same time. Hence, the memory structure of the present invention is much simplified than the prior art. The present invention also effectively compresses the data so that the size of the frame memory can be reduced. The present invention also uses alternate reading/writing and interpolation by using the adjacent pixels to further reduce the size of the frame memory (less than 1/2 of the conventional frame memory).

[0026] The above is a brief description of some deficiencies in the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims.

Brief Description of Drawings

[0027] FIG. 1 is a pixel of a conventional LCD.

[0028] FIG. 2 shows the relationship between the voltage applied to the liquid crystal capacitor of a pixel |V| and the frame time.

[0029] FIG. 3 shows the relationship between the gray level and the frame time for a pixel.

[0030] FIG. 4 shows the conventional method to improve the response delay on the LCD.

[0031] FIG. 5 shows the relationship between the gray level and the frame time for a pixel after the conventional method in FIG. 4 is applied.

[0032] FIG. 6 is a block diagram of a circuit for enhancing the motion picture quality in accordance with a preferred embodiment of the present invention.

[0033] FIG. 7 is a block diagram of a circuit for enhancing the motion picture quality in accordance with another preferred embodiment of the present invention.

DETAILED DESCRIPTION

[0034] FIG. 6 is a block diagram of a circuit for enhancing the motion picture quality in accordance with a preferred embodiment of the present invention. The circuit includes a nonlinear quantizer 610, data latches 620 and 640, dual-port buffers 632 and 634, a multiplexer unit 636, a frame memory 638, a motion picture enhancing unit 652,and a data processing unit 654. This circuit can be applied to a LCD.

[0035] When playing a motion video, the nonlinear quantizer 610 receives a frame data 602 from a previous-level circuit such as image decoder. The frame data 602 is, for exam-

ple, a 108 MHz stream data having RGB colors, and each color uses 8 bits to represent the data. The frame data 602 is converted by using a nonlinear quantization method to a frame data 611. The frame data 611 is, for example, a 108 MHz stream data having RGB colors, and each color uses 5 bits to represent the data. The nonlinear quantizer 610 can be implemented by a random only memory (ROM). The frame data 602 is inputted into the ROM as an address signal to read the quantized value stored in the ROM. This quantized value is the frame data 611.

[0036] The data latch 620 receives the frame data 611 from the nonlinear quantizer 610 and outputs the frame data 621. The frame data 621 is, for example, a 54 Mbps stream data having RGB colors, and each color uses 10 bits to represent the data. In this embodiment, the number of bits of the frame data 621 is 10; the number of bits of the frame data 611 is 5. That is, the number of bits of the frame data 621 is integral of the number of bits of the frame data 611.

[0037] The dual-port buffer 632 receives and temporarily stores the frame data 621, and outputs the frame data 631 based on the first-in-first-out rule. The frame data 631

is, for example, a 108 Mbps stream data having RGB colors, and each color uses 10 bits to represent the data. The dual-port buffer 634 receives and temporarily stores the frame data 635, and outputs the frame data 637 based on the first-in-first-out rule. The frame data 635 is, for example, a 108 Mbps stream data having RGB colors, and each color uses 10 bits to represent the data. The frame data 637 is, for example, a 54 Mbps stream data having RGB colors, and each color uses 10 bits to represent the data. The frame data 631 is shown in a motion picture after the frame data 635. The frame memory 638 stores the motion picture data. The multiplexer unit 636 is coupled to the dual-port buffers 632 and 634, and the frame memory 638. The multiplexer unit 636 will select to transmit the frame data 631 outputted from the buffer 632 to the frame memory 638, or transmit the frame data 635 outputted from the frame memory 638 to the buffer 634, based on the reading/writing time sequence.

[0038] This embodiment further includes data path controller (not shown) to control the reading/writing time sequence of the frame data 635, and the dual-port buffer 632 and 634, which makes the multiplexer unit 636 switch according to the time sequence of the memory. The clock signal

for inputting/outputting data and the control signal of the data path controller for controlling the frame data 635 can be the same as the those for controlling the frame data 602; e.g., 108Mbps. To match the time sequence of the data path controller for reading/writing, the size of the dual-port buffers 632 and 634 can be determined by the following equation: Size of the buffer < 2 x Delay for switching reading/writing x Number of switching x Data bandwidth.

[0039] The data latch 640 receives the frame data 637 from the dual-port buffer 632 and outputs the frame data 641. The frame data 641 is, for example, a 108 Mbps stream data having RGB colors, and each color uses 5 bits to represent the data. In this embodiment, the number of bits of the frame data 637 is 10; the number of bits of the frame data 641 is 5. That is, the number of bits of the frame data 637 is integral of the number of bits of the frame data 641.

[0040] The motion picture enhancing unit 652 simultaneously receives the frame data 611 and 641, and generates the compensation data 651 according to the difference between the frame data 611 and 641. This motion picture enhancing unit 652 can be implemented by a look-up ta-

ble. The data processing unit 654 compensates the corresponding frame data 602 in response to the compensation data 651 to obtain the frame data 604. The frame data 604 is then sent to the next-level circuit.

[0041] In a second embodiment of the present invention, even if the nonlinear quantizer 610 and the motion picture enhancing unit 652 in FIG. 6 are not used so that the frame data 602 and 611 are the same signal, and the frame data 641 and 651 are the same signal, this circuit is still within the scope of the present invention. In a third embodiment of the present invention, the circuit omits the data latches 620 and 640 in the second embodiment, this circuit is still within the scope of the present invention. In addition, the signal converter 650 can also be replaced by the other units in the above embodiments.

[0042] Referring to FIG. 6, the fourth embodiment of the present invention is illustrated as follows. This circuit is similar to the circuit described in the first embodiment except that the memory structure of the frame memory module 630 is replaced with another structure. In the fourth embodiment of the present invention, the frame memory module 630 can be any structure having the ability to store the present frame data and output the previous frame data at the

same time. In a fifth embodiment of the present invention, the data latches 620 and 640 in the fourth embodiment can be omitted.

[0043] The present invention also uses alternate reading/writing and interpolation by using the adjacent pixels to further reduce the size of the frame memory. FIG. 7 is a block diagram of a circuit for enhancing the motion picture quality in accordance with the sixth embodiment of the present invention. The circuit includes data flow switchers 710 and 780, nonlinear quantizers 720 and 730, data latches 740 and 760, dual-port buffers 752 and 754, a multiplexer unit 756, a frame memory 758, a motion picture enhancing unit 772, and data processing units 774 and 776. This circuit can be applied to a LCD.

[0044] In this embodiment, when playing the motion video, the data flow switcher 710 receives the frame data from the previous-level circuit such as an image decoder and separates the frame data into odd frame data 701 and even frame data 702 according to the order of the stream. The frame data 701 and 702 are for example 54 MHz stream data having RGB colors, and each color uses 8 bits to represent the data. The data flow switcher 710 receives the frame data 701 and 702 and introduces them to be one of

frame data 713 and 711 respectively.

[0045] The nonlinear quantizer 720 receives the frame data 713 and converts it by using a nonlinear quantization method to a frame data 721. The frame data 721 is, for example, a 54 MHz stream data having RGB colors, and each color uses 5 bits to represent the data. The nonlinear quantizers 720 and 730 can be implemented by random only memory. The frame data 713 and 711 are inputted into the ROM as address signals to read the quantized values stored in the ROM. The quantized values are the frame data 721 and 731.

[0046] The data latch 740 receives the frame data 721 and outputs the frame data 741. The frame data 741 is, for example, a 27 MHz stream data having RGB colors, and each color uses 10 bits to represent the data. That is, the number of bits of the frame data 741 is integral of the number of bits of the frame data 721.

[0047] The dual-port buffer 752 receives and temporarily stores the frame data 741, and outputs the frame data 751 based on the first-in-first-out rule. The frame data 631 is, for example, a 54 MHz stream data having RGB colors, and each color uses 10 bits to represent the data. The dual-port buffer 754 receives and temporarily stores the

frame data 755, and outputs the frame data 757 based on the first-in-first-out rule. The frame data 757 is, for example, a 27 Mbps stream data having RGB colors, and each color uses 10 bits to represent the data. The frame data 755 is, for example, a 54 MHz stream data having RGB colors, and each color uses 10 bits to represent the data. The frame data 751 is shown in a motion picture after the frame data 757. The frame memory 758 stores the motion picture data. The multiplexer unit 756 is coupled to the dual-port buffers 752 and 754, and the frame memory 758. The multiplexer unit 756 will select to transmit the frame data 751 outputted from the buffer 752 to the frame memory 758, or transmit the frame data 753 outputted from the frame memory 758 to the buffer 754, based on the reading/writing time sequence.

[0048] The data latch 760 receives the frame data 757 and outputs the frame data 761. The frame data 761 is, for example, a 54 Mbps stream data having RGB colors, and each color uses 5 bits to represent the data. That is, the number of bits of the frame data 757 is integral of the number of bits of the frame data 761.

[0049] The motion picture enhancing unit 772 simultaneously receives the frame data 731 and 761, and generates the

compensation data 771 according to the difference between the frame data 731 and 761. This motion picture enhancing unit 772 can be implemented by a look-up table. The data processing unit 774 compensates the corresponding frame data 713 in response to the compensation data 771 to obtain the frame data 773. The data processing unit 776 compensates the corresponding frame data 711 in response to the compensation data 771 to obtain the frame data 775. The data flow switcher 780 receives the frame data 775 and 773 and introduces them to be one of the frame data 704 and 703 respectively. The frame data 703 is the compensated odd frame data; the frame data 704 is the compensated even frame data. After combining the frame data 704 and 703, the combined frame data can be sent to the next-level circuit such as image driving circuit.

[0050] In a seventh embodiment of the present invention, even if the nonlinear quantizers 720 and 730, and the motion picture enhancing unit 772 in FIG. 7 are not used so that the frame data 713 and 721 are the same signal, and the frame data 761 and 771 are the same signal, this circuit is still within the scope of the present invention. In an eighth embodiment of the present invention, the circuit omits the

data latches 740 and 760 in the seventh embodiment, the frame data 713 and 741 are the same signal and the frame data 757 and 761 are the same signal; this circuit is still within the scope of the present invention. In addition, the signal converter 770 can also be replaced by the other units in the above embodiments.

[0051] Referring to FIG. 7, the ninth embodiment of the present invention is illustrated as follows. This circuit is similar to the circuit described in the sixth embodiment except that the memory structure of the frame memory module 750 is replaced with another structure. In the ninth embodiment of the present invention, the frame memory module 750 can be any structure having the ability to store the present frame data and output the previous frame data at the same time. In a tenth embodiment of the present invention, the data latches 740 and 760 in the ninth embodiment can be omitted.

[0052] In the sixth, seventh, ninth, and tenth embodiments, the data processing units 776 and 774 compensate the frame data 711 and 713 with a same compensation data 771. But the frame data 713 also can be compensated according to the difference between the frame data 711 and 713.

[0053] The above description provides a full and complete description of the preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is defined by the following claims.